CLAIMS

What is claimed is:

1. A system comprising:

first and second modules;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first path of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector and to the second module;

wherein the first path in the first module couples to stubs for first and second chips of the first module and the first path in the second module couples to stubs for first and second chips of the first module; and

each of the first and second chips include selectable on die terminations and wherein the on die terminations of the first and second chips of the first module are disabled and the on die terminations of the first and second chips of the second module are enabled.

2. The system of claim 1, wherein the first path in the first module is coupled to the stubs for the first and second chips through longer stubs.

3. The system of claim 1, wherein the first path in the first module includes a short loop through section and the first path in the second module does not include a short loop through section.

4. The system of claim 1, wherein each of the on die terminations include multiple R-termination elements which may be individually enabled or disabled.

5. The system of claim 4, wherein the number of R-termination elements selected in an enabled on die termination is chosen to select a desired impendence.

6. The system of claim 1, wherein there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path and the additional paths couple to stubs for chips with selectable on die terminations.

7. The system of claim 1, further comprising:

a second path of conductors extending from the circuit board to the second module connector, to the second module, back to the second module connector, to the circuit board, to the first module connector and to the first module;

wherein the second path in the second module couples to stubs for third and fourth chips of the second module and the second path in the first module couples to stubs for third and fourth chips for the second module; and

each of the third and fourth chips include selectable on die terminations and wherein the on die terminations of the third and fourth chips of the second module are disabled and the on die terminations of the third and fourth chips of the first module are enabled.

8. The system of claim 7, wherein the first path in the first module is coupled to the stubs for the third and fourth chips through longer stubs.

9. The system of claim 7, wherein the first path in the first module includes a short loop through section and the first path in the second module does not include a short loop through section.

10. The system of claim 7, wherein there are additional paths having a path like that of the third path and other additional paths having a path like that of the fourth path and the additional paths couple to stubs for chips with selectable on die terminations.

11. The system of claim 7, further comprising a controller coupled to the first and second paths.

12. The system of claim 7, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the back side of the second module.

13. The system of claim 7, wherein the first and second module connectors each have front sides and back sides, and the first path extends from the back side of the first module to the front side of the second module.

14. The system of claim 7, wherein the system includes X paths including the first and second paths, and the first and second modules each include 2X chips and wherein each of

the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module.

15. The system of claim 1, further comprising a buffer on the first module and a buffer on the second module.

16. The system of claim 1, further comprising error correction code chips on the first module and error correction code chips on the second module.

17. The system of claim 1, wherein the circuit board is a printed circuit board and a motherboard.

18. The system of claim 1, wherein impedances of the paths in the first module are at least 50% higher than the paths on the circuit boards.

19. The system of claim 1, wherein there is an additional module between module 1 and module 2.

20. A system comprising:

first and second modules;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first data path of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, and to on module terminations of the second module, wherein the first path in the first module is connected to stubs with in turn are coupled to stubs of first and second chips of the first module; and

a second data path of conductors extending from the circuit board to the second module connector, to the second module, back to the second module connector, to the circuit board, to the first module connector, to the first module, and to on module terminations of the first module, wherein the second path in the second module is connected to stubs with in turn are coupled to stubs of first and second chips of the second module.

21. The system of claim 20, wherein there are module connector connections between the circuit board and the first and second module connectors on the path.

22. The system of claim 20, wherein there are additional paths having a path like that of the first path and other additional paths having a path like that of the second path.

23. The system of claim 20, wherein there are module connector connections between the circuit board and the first and second module connectors on the path.

24. The system of claim 20, wherein the first and second module connectors are keyed such that a similarly keyed module can be inserted in only one orientation into the corresponding module slot.

25. A system comprising:

first and second modules;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first path of conductors extending from the circuit board to the first module connector, to the first module, back to the first module connector, to the circuit board, to the second module connector, to the second module, to an on module termination of the second module, wherein a first section of the first path, which is a short loop through section, couples to stubs for first and second chips of the first module, and a second section of the first path couples to stubs for first and second chips of the second module; and

a second path of conductors extending from the circuit board to the second module connector, to the second module, back to the second module connector, to the circuit board, to the first module connector, to the first module, to an on module termination of the first module, wherein a first section of the second path, which is a short loop through section, couples to stubs for third and fourth chips of the second module and a section of the second path couples to stubs for third and fourth chips of the first module.

26. The system of claim 25, wherein the system includes

X paths including the first and second paths, and

the first and second modules each include 2X chips including the first, second, third, and fourth chips of the first and second modules, and wherein each of the X paths couples to stubs for a different two of the 2X chips of the first module and for a different two of the 2X chips of the second module.

27. The system of claim 25, wherein the first and second modules and first and second module connectors are keyed so as to be able to be received by the modules in only one orientation.

28. The system of claim 25, wherein the first and second modules are interchangeable so that the first module may be received by the second module connector and the second module received by the first module connector without rotating the orientation of either module.

29. The system of claim 25, wherein there are additional paths having a path like that of the first path and other additional paths following a path like that of the second path.

30. A DRAM comprising:

a stub to pass data;

a load; and

selectable on die termination coupled to the stub and load.

31. The DRAM of claim 30, wherein the on die termination include multiple R-termination elements which may be individually enabled or disabled.